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31. (Amended) A computer system comprising:

at least one processor;

a system bus;

a memory device coupled to the system bus, the memory device including one or more memory cells comprising:

a substrate;

a drain formed in the substrate;

a source rail formed in the substrate;

a first oxide layer deposited over the substrate stretching from the drain to the source rail;

a silicon-containing barrier layer deposited over the first oxide layer said barrier layer comprising a silicon-containing material from a precursor layer, previously deposited over at least a portion of said first electrode, that has been reacted with a reactive agent; and

a gate electrode deposited over the silicon-containing barrier layer.

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32. (New) A device comprising:

a substrate including at least one semiconductor layer;

a semiconductor device fabricated proximate to the substrate; and

a barrier layer formed from a silicon source previously deposited over at least a portion of the semiconductor device, having been reacted with a reactive agent.

33. (New) The device of claim 32, wherein the silicon source is a silazane.

34. (New) The device of claim 32, wherein the silicon source is selected from the group comprising hexamethyldisilazane, tetramethyldisilazane, octamethylcyclotetrasilazane, hexamethylcyclotrisilazane, diethylaminotrimethylsilane and dimethylaminotrimethylsilane.

35. (New) The device of claim 32, wherein the silicon-containing material is from a silane source.

36. (New) The device of claim 32, wherein the reactive agent is selected from the group comprising NH_3 , N_2 , O_2 , O_3 , N_2O and NO .

37. (New) The device of claim 32, wherein the barrier layer is primarily nitride.

38. (New) The device of claim 32, wherein the barrier layer is primarily oxide.

39. (New) The device of claim 32, wherein the barrier layer is primarily oxynitride.

40. (New) A device having a barrier layer comprising:

- a substrate including at least one semiconductor layer;
- a first semiconductor device fabricated proximate to said substrate;
- a silicon-containing material, previously formed over at least a portion of said first semiconductor device, that has been reacted with a reactive agent to form a barrier layer; and
- a second semiconductor device formed over said barrier layer.

41. (New) The method of claim 40, wherein the reactive agent is NH_3 and the barrier layer is primarily nitride.

42. (New) A device having a barrier layer comprising:

- a silicon substrate including at least one semiconductor layer;
- a silicon-containing material from a silazane source, previously formed over at least a portion of said silicon substrate, that has been reacted with a reactive ambient to form said barrier layer.

43. (New) A semiconductor device having a barrier layer comprising:

- a substrate having at least one semiconductor layer;
- a transistor structure formed proximate to said substrate, said transistor structure including
 - a source formed in said substrate,
 - a drain formed in said substrate, and

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a gate oxide layer formed over an active area between said source and drain; and
a silicon-containing material, previously formed over at least a portion of the
transistor structure, that has been reacted with a reactive agent to form the barrier layer.

44. (New) The device of claim 43 wherein a gate electrode is formed over said barrier layer.

45. (New) The device of claim 43, wherein said gate electrode is doped with phosphor.

46. (New) The device of claim 43, wherein said gate electrode is doped with boron.

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47. (New) The device of claim 43, wherein said reactive agent comprises an oxidizing agent
which causes silicon atoms of the silicon-containing material to bond with oxygen atoms of the
oxidizing agent.

48. (New) A capacitor device comprising:

an electrode formed over a substrate;

a silicon-containing material, from a precursor layer previously formed over the
electrode, that has been processed using rapid thermal nitridation with a nitridizing reactant to
form a barrier layer; and

a dielectric layer formed over said barrier layer.

49. (New) A semiconductor device having a barrier layer containing no metal comprising:

a substrate including at least one semiconductor layer; and

a silicon-containing material, from a silicon source previously formed over at least a
portion of the semiconductor device, that has been reacted with a reactive agent to form said
barrier layer containing no metal.

50. (New) A semiconductor device having a barrier layer containing no metal comprising:

a silicon substrate including at least one semiconductor layer; and

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a silicon-containing material, from a silazane source previously formed over at least a portion of the silicon substrate, that has been reacted with a reactive agent to form said barrier layer containing no metal.

51. (New) A semiconductor device having a barrier layer containing no metal comprising:

a substrate having at least one semiconductor layer;

a transistor structure formed proximate to said substrate, said transistor structure including:

a source formed in said substrate,

a drain formed in said substrate, and

a gate oxide layer formed over an active area between said source and drain; and

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a silicon-containing material, previously formed over at least a portion of the transistor structure, that has been reacted with a reactive agent to form said barrier layer containing no metal.

52. (New) A capacitor device with a barrier layer containing no metal comprising:

an electrode formed over a substrate;

a silicon-containing material, previously formed over said electrode, wherein said silicon-containing material has been processed using rapid thermal nitridation with a nitridizing reactant to form the barrier layer containing no metal; and

a dielectric layer formed over said barrier layer.

53. (New) A capacitor device comprising:

a first electrode formed over a substrate;

a silicon-containing barrier layer formed over at least a portion of said first electrode, said barrier layer comprising a silicon-containing material from a precursor layer previously deposited over at least a portion of said first electrode from a silicon source, reacted with a reactive agent selected to react with silicon of the silicon-containing material;

a dielectric layer formed over said silicon-containing barrier layer; and

a second electrode formed over the dielectric layer.

54. (New) The capacitor device of claim 53, wherein the silicon source is a silazane.

55. (New) The capacitor device of claim 53, wherein the silicon source is selected from the group comprising hexamethyldisilazane, tetramethyldisilazane, octamethylcyclotetrasilazane, hexamethylcyclotrisilazane, diethylaminotrimethylsilane and dimethylaminotrimethylsilane.

56. (New) The capacitor device of claim 53, wherein the silicon-containing material is from a silane source.

57. (New) The capacitor device of claim 53, wherein the reactive agent is selected from the group comprising NH_3 , N_2 , O_2 , O_3 , N_2O and NO .

58. (New) The capacitor device of claim 53, wherein the barrier layer is primarily nitride.

59. (New) The capacitor device of claim 53, wherein the barrier layer is primarily oxide.

60. (New) The capacitor device of claim 53, wherein the barrier layer is primarily oxynitride.

REMARKS

Claims 30-31 have been rejected. Applicants have added claims 32-60, thus claims 30-60 are pending in the present application. Applicants acknowledge that the oath/declaration is acceptable.

Drawings

The Examiner has objected to the drawings. Specifically, Fig. 4 does not correspond with reference sign 401 in the specification on page 10, line 6. A new Fig. 4 is being submitted with this paper. New Fig. 4 contains the appropriate reference sign 401 in place of the inappropriate reference sign 407. A marked up version of Fig. 4 is also being submitted with this paper to show the changes made.